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**IBM**

7 clock when the machine is being cycled down to failure and  
the major change needing re-calibration is cycle time.

1 Claim 13. (Previously submitted) The method of claim 5  
2 wherein a state machine controls calibration, and said state  
3 machine allows  
4 a. putting the system of the interface into a wait state and  
5 for quiescing the data over the bus interface when the state  
6 machine enters a re-calibration state, whereupon,  
7 b. said a fast initialization process for calibration is  
8 performed, and then  
9 c. a change of said ~~state~~ state machine takes the system of  
10 the bus interface back out of said wait state; and  
11 d. allows data to transfer across the bus interface again.  
12

### REMARKS/ARGUMENTS

The examiner's extensive review of the references and claims is appreciated.

Applicants remind the Examiner that in the last response, it was said:

"The amendments to the claims include changes made of an editorial nature which should not be construed to limit the claimed invention, but the limitation relating to the quiesce wait state is a limitation made to distinguish the invention from the art put together without justification in the first rejection. Reconsideration of the application in light of these amended claims is requested.

As indicated in the description of the background of the art, there was no way to recalibrate prior interfaces once an interface was up and running. This is because sending calibration patterns across the interface would interfere with system operations. Also, cumulative degradations could eventually cause a system failure. Nothing in the art recognized the deficiencies and its cause.

The claim includes the limitation "SMP computer system with a system quiesce operation having a source-synchronous, pipelined, self-calibrating bus interface" but the primary reference

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does not deal with an SMP source-synchronous, pipelined, self-calibrating interface, but rather the clock timing of a memory chip. The blocking of input and output data at the interface in the primary reference is locally generated by the interface controls when clocks are not synchronized. In an SMP system, unlike atomic memory operations, data cannot always be fenced without regard to system effects. The primary reference does not address any solution for that problem. Neither does the primary discuss sending any calibration patterns sent on the interface.

Nuckolls (of the previous rejection) on the other hand stops all clocks, and does not deal with a running SMP computer system that is quiesced while a calibration is done. While the Nuckolls system is stopped it does nothing. The claimed invention does calibration of the data interface during the quiescent state. There is nothing in the references that even suggests this should be done, let alone teach how to do it."

Now the Examiner has done still another search and come up with a new reference and combine that new reference which is inapplicable with applicants admitted Prior Art (US 6654897 granted 2003/11/15) as described on page 4 of the application to provide a basis for the current final rejection. The other new primary reference is Intel's 5613071. The applicants believe that one skilled in this art should know that Intel did not provide an elastic interface in the last decade and none is described in 5613071. Applicants Assignee's 6654897 does provide an elastic interface, as do the systems of others in the industry that are licensed to use US 6654897. However, all of these systems, as described in the application itself provided no way to re-calibrate an interface once it was up and running.

And that is true of the current reference tried by the Examiner again in the Final rejection. The applicants are careful to present their view as to the art and appreciate examinations of these applications. However, again the Examiner has missed the point.

Please enter this amendment no to place this case in condition for allowance or for the purpose of appeal.

Allowance is appropriate. The claims 1-12 stand rejected under 35 USC 103(a) as being unpatentable over US 5613017 to Rankin et al, in view of Applicants Admitted Prior Art (APA, also known as US 6654897)

In summary, under 35 USC 103(a) the claims 1-12 stand rejected as being unpatentable over the US5613017 (which has no elastic interface and is unrelated to any hardware that has the problem that the applicant's invention overcomes in light of an IBM reference which has the problem that none previously had understood or solved.

It is the applicant's position that this rejection is untenable.

Further, the Examiner misunderstands and mischaracterizes the art he has used.

Patent 5,613,071 to Rankin, et al. is referenced in regard to claim 1-12 which include the following steps:

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- a) halting operations of said SMP computer system having a source-synchronous, pipelined, self-calibrating bus interface with a system quiesce operation such that the bus interface is not used by the system,
- b) fencing a receiver of the bus interface,
- c) recalibrating the bus interface using clock readjustment,
- d) unfencing the receiver of the bus interface, and
- e) taking the system of the bus interface out of a the (as amended here) wait state and commencing operations to allow interface use again.

The examiner references recalibration of an interface [58] with the steps of fencing the interface [col. 8, lines 50-62], recalibrating the interface for synchronization [col. 8, lines 58-60], and unfencing the interface [col. 8, lines 50-62]. Now the examiner ignores the teaching of 5613071 in many respects. Firstly, the description is of an MPP system consisting of many nodes having a local processor while trying to maintain the shared memory style of programming used in SMP systems. The claims requires an SMP computer system, not an MPP computer system. The Examiner ignores this. Furthermore, the claim requires a source-synchronous, pipelined, self-calibrating bus interface with a system quiesce operation such that the bus interface is not used by the system. The Rankin system does not have this. So, the base premise that the examiner submits, that the primary reference has the bus interface of the applicant is not factually correct. Furthermore, there is no teaching of fencing a receiver of a nonexistent bus interface, nor recalibrating the non existent self calibrating bus interface with a system quiesce operation for synchronization, nor unfencing such an interface.

Basically, the inventors contend that Rankin does not teach the claimed aspects of this application, or even the basic system that has the problem that the inventors now recognize have a problem to be fixed. First of all, Rankin points out that the remote node hardware is very performance-optimized. The two impacts on software mentioned are [col. 8, 37-49].

1. Writes to remote memory are acknowledged prior to actually occurring. Instead, they are acknowledged when they enter the queue.
2. The writes/requests may be completed in any order.

It is for these two reasons, that the text mentions the programmer may need to make program modifications to support 'data consistency' [col. 8, 49]. Rankin goes on to mention how this can be done through memory fences [col. 8, lines 50-62]. Memory fences are not what the applicants have claimed. Furthermore, the term 'synchronization' refers to a **software synchronization** and does not refer to **interface recalibration**. It is what the **programmer may need**, not what the **hardware requires**. There is a big difference. Throughout that section, there is no mention about what the **hardware may need**, only hardware symptoms that the **programmer may need** to be aware of.

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Rankin makes no mention of the need to stop using the interface in order to make any hardware adjustments on the interface itself. It also does not teach or even mention that memory fencing may have a **side benefit** of allowing recalibration. In fact, nowhere does it mention that the interface needs **any maintenance**, including the need to recalibrate the interface for reasons of drift.

Furthermore, 'data consistency' is different from 'halting operations of the SMP' and making sure the interface is 'idle' with the claimed system quiesce operation. The term 'data consistency' only implies that memory coherency be maintained **within a particular application or group of programs**. The description mentions the user's program or application. It does not discuss the need to do this for **ALL programs simultaneously**. In other words, some applications may need memory fencing while others may not. So, while some programs are doing the software synchronizing or other locking needed by those programs, other programs could be using the interface. This would not satisfy the requirements of the recalibration sequence claimed in the claims of this application.

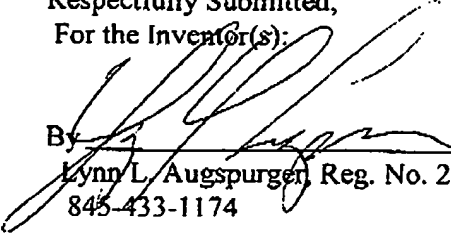
The system level 'halting' provided by a system quiesce operation guarantees that the source-synchronous, pipelined, self-calibrating bus interface is not used for non memory-coherent operations as well as all memory-coherent operations - **it is truly idle from a system perspective**.

Rankin does not even provide the first step of the claimed invention with a system level "halting" of the source-synchronous, pipelined, self-calibrating bus interface. Rankin does not even recognize that there is a need to be solved. Only at the **operating system level or global software management level** can this be accomplished by Rankin if his system had applicant's bus interface, which it does not. Rankin does not mention the need for this level of control nor how to accomplish it.

Each claim is believed independently patentable, and Rankin, alone, or Rankin coupled with a system which has a problem which is not solved, does not teach these applicant's claimed inventions.

It is believed that this application now stands in condition for allowance. A notice of allowance is now respectfully requested.

Respectfully Submitted,  
For the Inventor(s):

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845-433-1174

Date: 3/10/2005

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